ACHARYA INSTITUTE OF TECHNOLOGY

Acharya Dr.Sarvepalli Radhakrishnan Road,Bangalore-560107

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Summer School
On
"Digital IC Design using Cadence Tools"
in
Association with
IEEE Student Branch,
Acharya Institute of Technology, Bangalore

Conducted by:

Department of Electronics and Communication Engineering

Acharya Institute of Technology

In

Association with

AIT Student Branch

&

SiyaCon Technologies

14th March to 25th March, 2023
VENUE:ECE Block

ACHARYA INSTITUTE OF TECHNOLOGY

IEEE BANGALORE SECTION

SilyaCon Technologies

Acharya Dr. Sarvepalli Radhakrishnan Road, Soladevanahalli, Hesaraghatta Main Road, Bengaluru- 560107

Summer School on "Digital IC Design using Cadence Tools" in Association with IEEE Student Branch, Acharya Institute of Technology, Bangalore

Date: 14-3-2023 to 25-3-2023 | Time: 9.30 am to 4.30 pm
Target Audience: ECE Students (Limited to 30 students only)
Venue: : VLSI Lab, ECE Department

ABOUT THE PROGRAM:

Objectives of the Program:

The summer school major goal is to give students hands-on experience with Cadence tools in order to simulate the development of cutting-edge technologies and methodologies for developing design excellence in the field of microelectronic system verification, design, and implementation, Advanced verification methodology, Analog mixed-signal design methodology, Design for test, Digital implementation, System-level design, Low-power methodology, RF design methodology, IP design, integration, and validation are all supported by the Cadence tool.

Expected Outcome of the Program:

- Build various digital logic gates using Cadence Tools.
- Design Schematic capture and perform functional simulation for various digital logic circuits.
- Analyze performance of designed logic gates in-terms of Area and Speed.

• Important Dates
Last date for registration: 11/3/2023

• Note:
1 .No Registration Fee
2. e-certificate will be provided for all participants

Registration Link/Form:
https://forms.gle/aDfWBcUU89y5xG639

ADVISORY COMMITTEE:
Dr. RAJATH HEGDE M.M
Principal, AIT, Bengaluru
Mr. MARIGOWDA C K
Vice Principal, AIT, Bengaluru
Dr. S K MURTHY
Patent Counsel,
Intel Technologies, Bengaluru
Dr. H V RAVISH ARADHYA
Professor, RV college of Engineering, Bengaluru
Dr. H C HANUMANTHRAJU
Professor, BMSIT, Bengaluru

CONVENERS:
Dr.RAJESWARI
Prof. and HOD Dept. of ECE, AIT

COORDINATORS:
Dr. JAYALAXMI H
Associate Prof, Dept of ECE, AIT
Dr. ASHA C.N
Associate Prof, Dept of ECE, AIT
Prof. NAGAPUSHPA K.P
Assistant Prof, Dept of ECE, AIT
Prof. VEENA SANATHKUMAR
Assistant Prof, Dept of ECE, AIT

Resource Persons

Dr. Jayalaxmi H
Associate Prof, Dept of ECE, AIT

Dr. Asha C.N
Associate Prof, Dept of ECE, AIT

Prof. Nagapushpa K.P
Assistant Prof, Dept of ECE, AIT
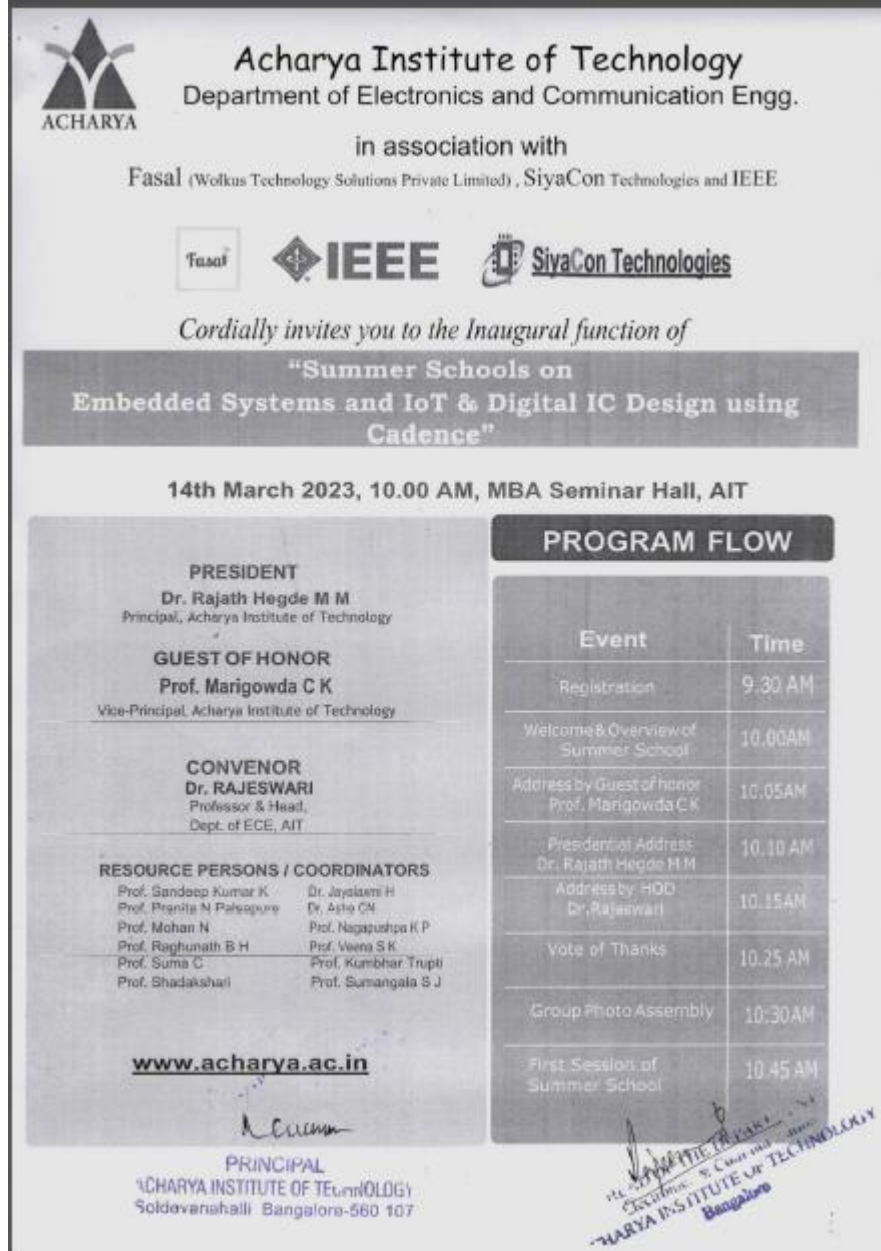
Prof. Veena Sanathkumar
Asst. Prof. Dept. of ECE

Technical Team: Mr. Vinod K R, Lab Instructor, Dept of ECE, AIT

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The Department of Electronics and Communication Engineering, Acharya Institute of Technology organized Summer School on "Digital IC Design using Cadence Tools" in Association with IEEE Student Branch, Acharya Institute of Technology, and SiyaCon Technologies, Bangalore for 6th semester students.

About the Program:

The summer school major goal is to give students hands-on experience with Cadence tools in order to simulate the development of cutting-edge technologies and methodologies for developing design

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excellence in the field of microelectronic system verification, design, and implementation, Advanced verification methodology, Analog mixed-signal design methodology, Design for test, Digital implementation, System-level design, Low-power methodology, RF design methodology, IP design, integration, and validation are all supported by the Cadence tool.

 No. of students attended the summer school:22

Registrations were open to all the students of 6th semester ECE using link

https://tinyurl.com/yyzuu2ne

Sessions were conducted offline with hands on approach to the students at VLSI Lab, ECE block.

Objectives of the event:

> ➤ To understand Digital IC Design Flow using Cadence Tools.

> ➤ To design Schematic Capture Analysis, Simulation for Various Logic Gates and its performance analysis using Cadence Tools.

Coordinators: Dr. Jayalaxmi H , Dr. Asha C.N, Prof. Nagapushpa K.P, Prof. Veena Sanath Kumar

Resource persons:

1 Dr. JayalaxmiH , Associate Prof, Dept of ECE,AIT
2 Dr. Asha C.N , Associate Prof, Dept of ECE,AIT
3 Prof. NagapushpaK.P ,Assistant Prof, Dept of ECE,AIT
4 Prof. Veena Sanath Kumar, Assistant Prof, Dept of ECE,AIT

Technical support: Mr.Vinod K R, Instructor Dept of ECE

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Topics included:

- Introduction to VLSI and CMOS Inverter Operation

- Custom IC Design Flow for Cadence Tool

- Schematic Capture Functional Simulation CMOS Inverter using Cadence Tools
- Schematic Capture Functional Simulation for NAND,NOR, EX-OR Logic Gates

- Schematic Capture Functional Simulation for Full Adder, Parallel Adder and Ripple Adder and its Timing Analysis

- Schematic Capture Functional Simulation for Multiplexers, Decoder and Encoders and its Timing Analysis

Expected Outcome of the Program:

- Build various logic gates using Cadence Tools.

- Design Schematic capture and perform functional simulation for various logic gates.

- Analyze performance of designed logic gates in-terms of Area and Speed.

Summer School was followed by Quizzes, Design Contest and Project based learning to evaluate the students.

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Some Photos taken during the event

Photo of the Inauguration of the Summer School by Dr. Rajeswari, Prof and Head, ECE Dept.

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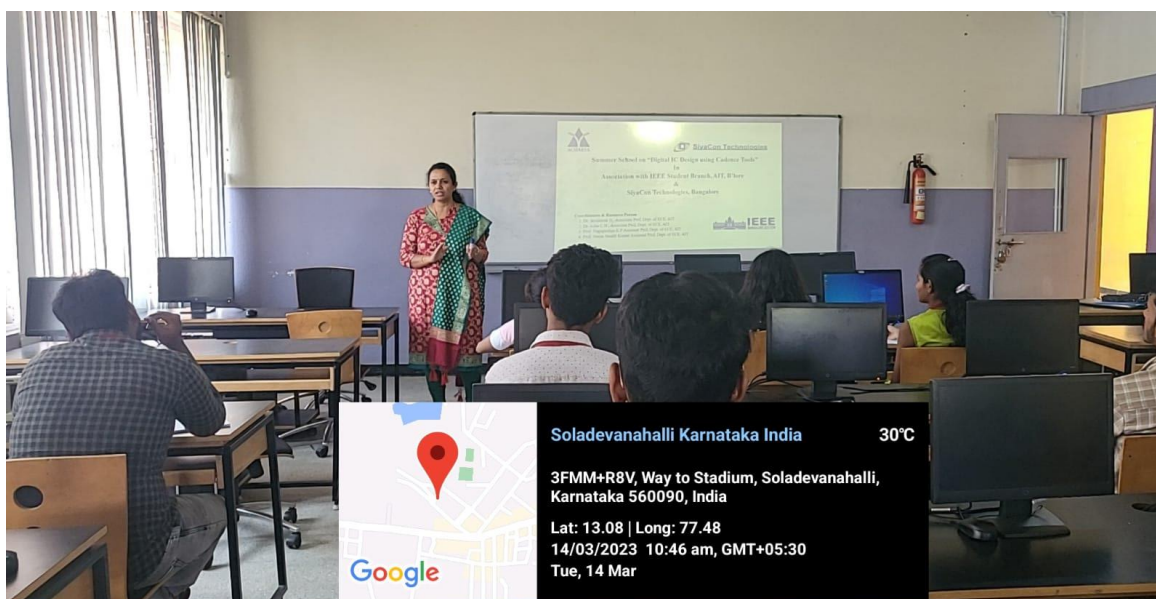**Photos taken during the session**
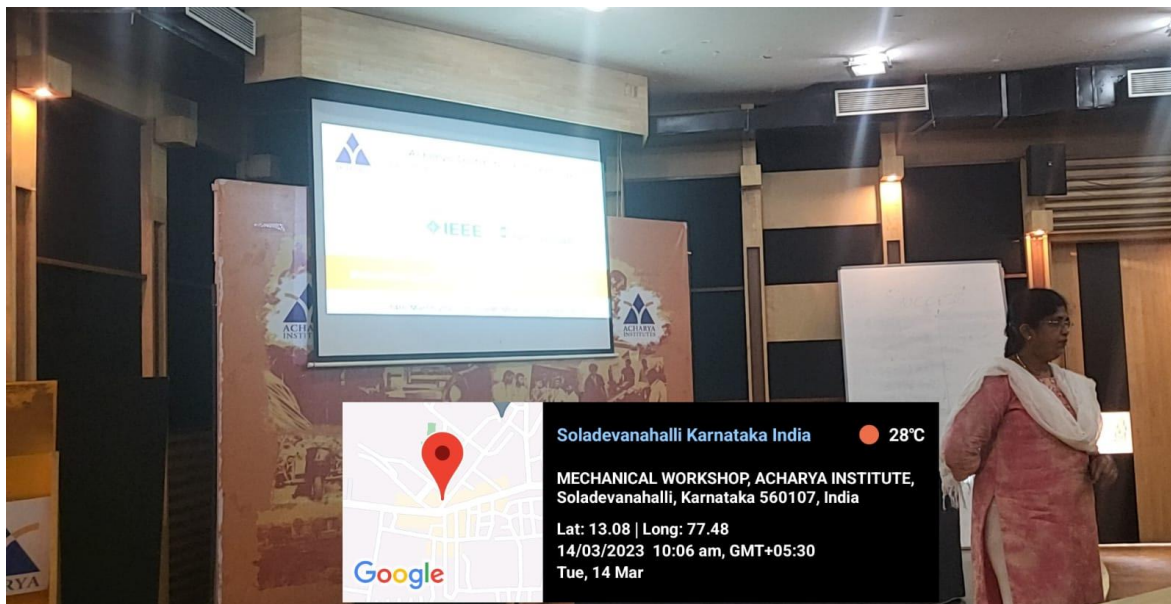
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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Soladevanahalli, 3FMJ+WVC, Acharya Dr Sarvepalli Radhakrishnan
Rd, Bengaluru, Karnataka 560107, India
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Long 77.481725°
16/03/23 10:35 AM GMT +05:30

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Photos taken during Students presentation on Project Based Learning
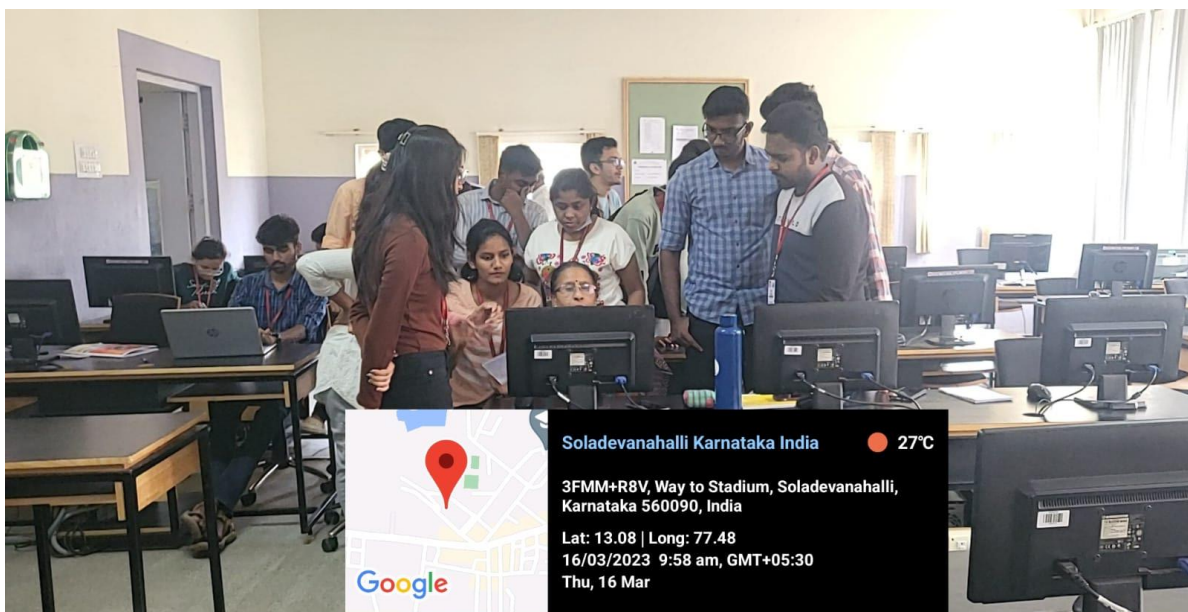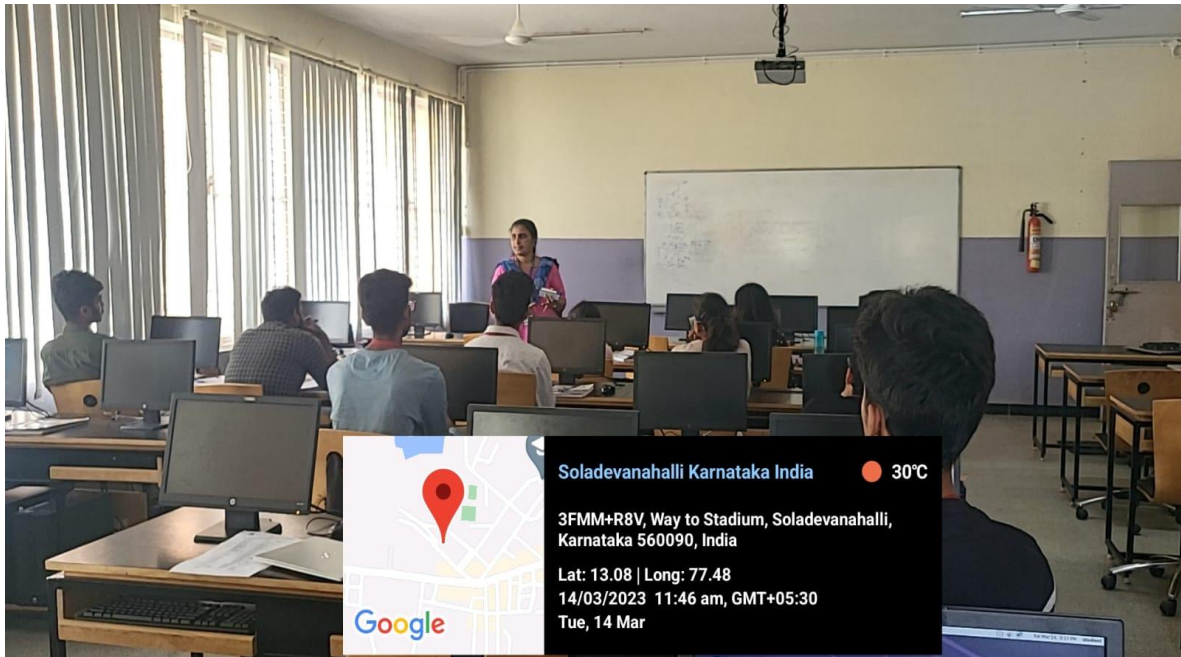
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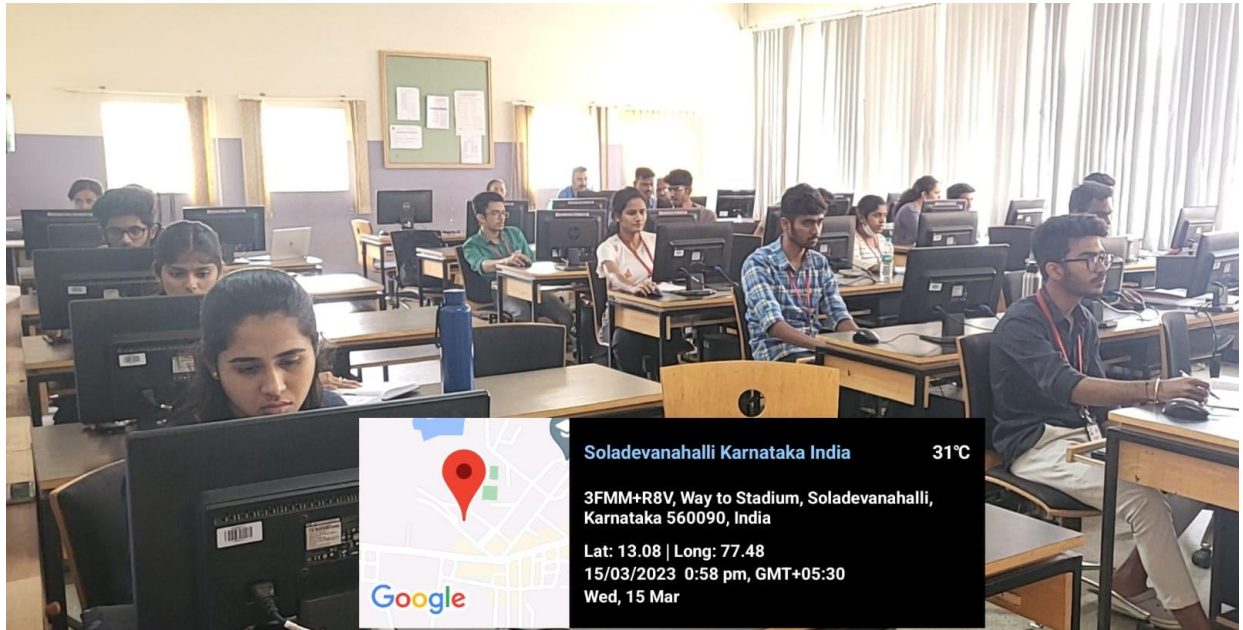Acharya Dr.Sarvepalli Radhakrishnan Road,Bangalore-560107

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Department of ECE   SiyaCon Technologies   IEEE BANGALORE SECTION

Summer School

"DIGITAL IC DESIGN USING CADENCE TOOLS"

Registration Form

Date : 14/03/2023 to 21/03/2023 and 24/03/2023 to 25/03/2023

Sl.No	Student Name
1	Abhishek K
2	Navashashank N
3	Abhishek L S
4	P Sai Prasanna Reddy
5	Tejas D Hunadre
6	Chandana R
7	Shashaka S
8	Goutham R
9	Harshini b s
10	Hemanth Kumar
11	Impana R Saini
12	Karthik V
13	Karunya Prakash
14	LikhitaJayakanth
15	Madan Kumar P
16	Meghana M S
17	Puneeth G
18	Shahid E
19	Sharadhi S K
20	Shreyas Jain R P
21	Swarna S S
22	Tejas D
23	Vikas P
24	Yashwanth Malviya
25	Bhavana
26	Tejas H

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IEEE AIT Student Branch   **SiyaCon**

Certificate of Participation

This certificate is presented to Ms. Chandana R for attending the Summer School on "Digital IC Design using Cadence Tools" from 14-03-2023 to 25-03-2023 conducted by Department of ECE in association with Siyacon Technologies, Bangalore and IEEE Student Branch at Acharya Institute of Technology, Bengaluru.

Dr. Rajeswari
H.O.D. Dept. of ECE
Acharya Institute of Technology

Prof. C K Marigowda
Vice-Principal
Acharya Institute of Technology

Dr. Rajath Hegde M M
Principal
Acharya Institute of Technology

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Certificate of Participation

This certificate is presented to Mr. Goutham D. G. for attending the Summer School on "Digital IC Design using Cadence Tools" from 14-03-2023 to 25-03-2023 conducted by Department of ECE in association with Siyacon Technologies, Bangalore and IEEE Student Branch at Acharya Institute of Technology, Bengaluru.

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This certificate is presented to Ms. Harshini B. S. for attending the Summer School on "Digital IC Design using Cadence Tools" from 14-03-2023 to 25-03-2023 conducted by Department of ECE in association with Siyacon Technologies, Bangalore and IEEE Student Branch at Acharya Institute of Technology, Bengaluru.

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IEEE
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Certificate of Participation

This certificate is presented to Mr. Hemanth Kumar for attending the Summer School on "Digital IC Design using Cadence Tools" from 14-03-2023 to 25-03-2023 conducted by Department of ECE in association with Siyacon Technologies, Bangalore and IEEE Student Branch at Acharya Institute of Technology, Bengaluru.

Dr. Rajeswari
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Prof. C K Marigowda
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Principal
Acharya Institute of Technology